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DATA SHEET

DIGITAL dcc COMPACT CASSETTE

SAA2032
Digital equalization for the tape drive processing of the DCC system

Product specification
Supersedes data of February 1993
File under Integrated Circuits, Miscellaneous

February 1995

Philips Semiconductors

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Digital equalization for the tape drive processing of the DCC system

SAA2032

FEATURES

- Analog-to-digital conversion, demultiplexing, equalization and zero crossing of time multiplexed analog read amplifier signal
- Microcontroller interface
- Search mode envelope, label and virgin detection of the AUX channel
- Search mode tape speed measurement
- Simplified external biassing
- Reduced power consumption
- Analog eye output
- 4 V nominal operating voltage capability.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

Performing the Digital Equalizing function in the Digital Compact Cassette (DCC) system, the SAA2032 is intended for use in conjunction with the SAA2022, read amplifier TDA1317 or TDA1318.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2032GP	44	QFP 1	plastic	SOT205AG

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *Quality Reference Pocketbook* are followed. The pocketbook can be ordered using the code 9398 510 34011.

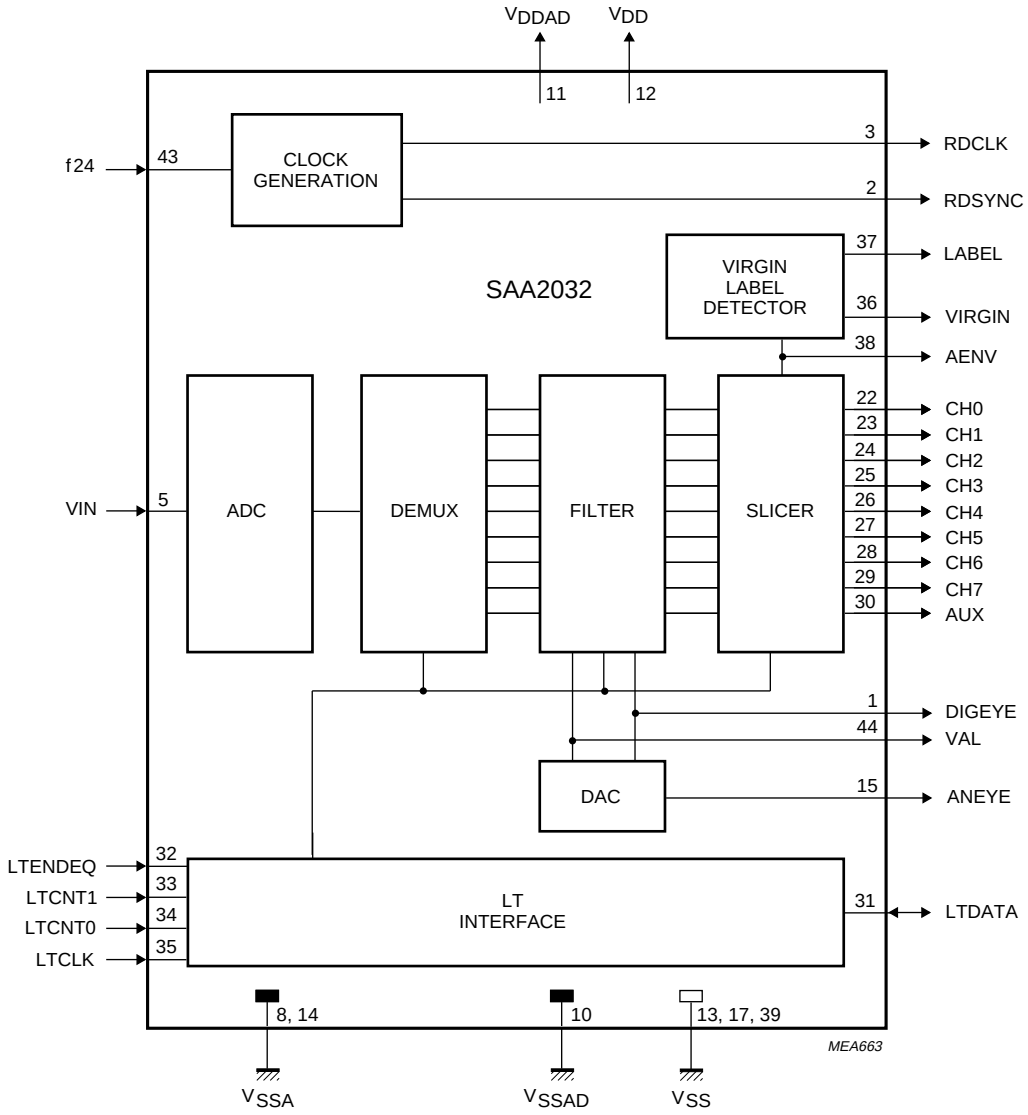


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DIGEYE	1	serial data output for eye pattern
RDSYNC	2	SYNC data for Read Amplifier (push-pull output)
RDCLK	3	data clock for Read Amplifier (push-pull output)
TEST1	4	test 1; to be connected to V_{SS}
VIN	5	analog time multiplexed input from Read Amplifier
REFN	6	lower reference voltage (+1 V) for ADC
REFP	7	upper reference voltage (+3.1 V) for ADC
V_{SSA}	8	analog ground (0 V)
BIASA	9	bias current for ADC (sinks current from V_{DDAD} via 33 kΩ)
V_{SSAD}	10	supply ground (0 V) for ADC
V_{DDAD}	11	supply voltage (+5 V) for ADC
V_{DD}	12	supply voltage (+5 V)
V_{SS}	13	supply ground (0 V)
V_{SSA}	14	supply ground (0 V)
ANEYE	15	analog eye voltage output
n.c.	16	not connected
V_{SS}	17	supply ground (0 V)
TEST4	18	test 4; do not connect
TEST5	19	test 5; do not connect
TEST6	20	test 6; do not connect
TEST7	21	test 7; do not connect
CH0	22	channel 0 output for SAA2022 (DCC Drive Signal Processing) (push-pull output)
CH1	23	channel 1 output for SAA2022 (push-pull output)
CH2	24	channel 2 output for SAA2022 (push-pull output)
CH3	25	channel 3 output for SAA2022 (push-pull output)
CH4	26	channel 4 output for SAA2022 (push-pull output)
CH5	27	channel 5 output for SAA2022 (push-pull output)
CH6	28	channel 6 output for SAA2022 (push-pull output)
CH7	29	channel 7 output for SAA2022 (push-pull output)
AUX	30	AUX channel output for SAA2022 (push-pull output)
LTDATA	31	microcontroller I/O data interface (3-state push-pull output and input; CMOS levels)
LTENDEQ	32	microcontroller interface enabling (CMOS input levels)
LTCNT1	33	microcontroller interface; mode control 1 (CMOS input levels)
LTCNT0	34	microcontroller interface; mode control 0 (CMOS input levels)
LTCLK	35	microcontroller bit-clock interface (CMOS input levels)
VIRGIN	36	search mode virgin detection output
LABEL	37	search mode label detection output
AENV	38	search mode auxiliary detection output
V_{SS}	39	supply ground (0 V)

SYMBOL	PIN	DESCRIPTION
TEST8	40	test 8 input; to be connected to V_{SS}
TEST9	41	test 9 input; to be connected to V_{SS}
TEST10	42	test 10 input; to be connected to V_{SS}
f24	43	clock input; typical frequency 24.576 MHz (CMOS input)
VAL	44	synchronization output for DIGEYE

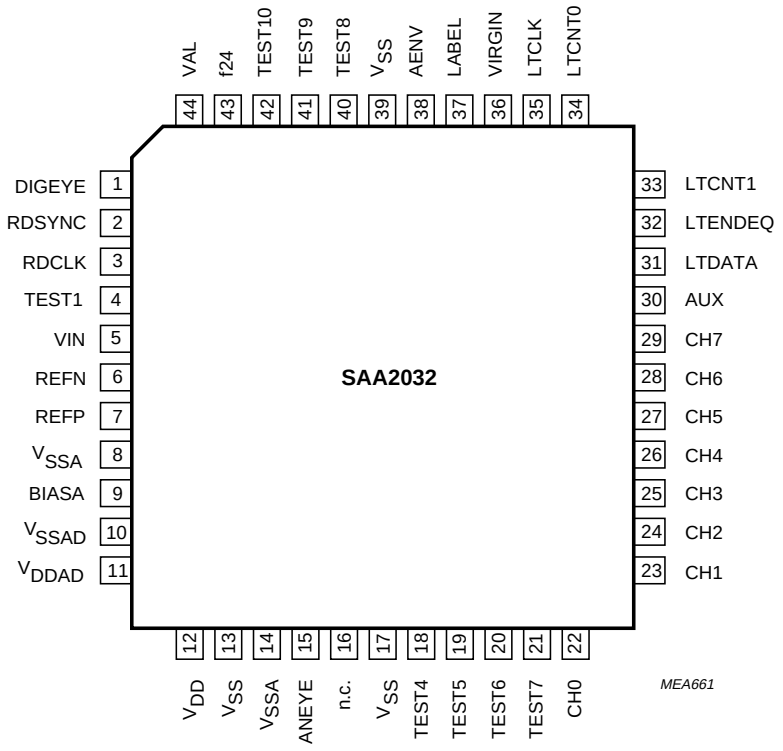


Fig.2 Pin configuration.

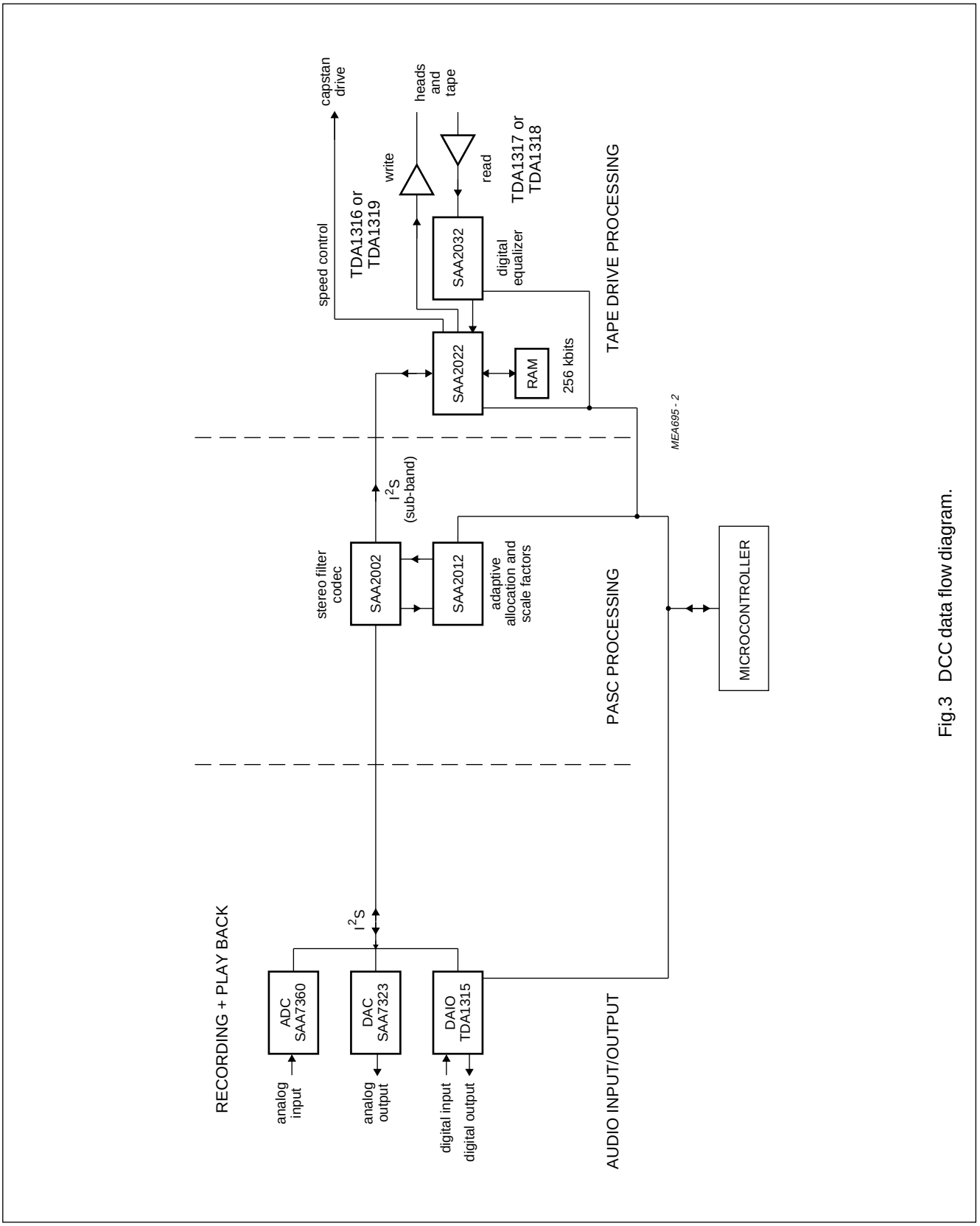


Fig.3 DCC data flow diagram.

FUNCTIONAL DESCRIPTION

Operating Modes

DEQ operating modes are programmed via the LT interface:

NORMAL

- A/D conversion
- Demultiplexing
- Equalization
- Zero crossing.

in this mode the SAA2032 performs the equalization and slicing of the eight data channels and the auxiliary channel. The eight data channels have a bit-rate of 96 kbits/s while the auxiliary channel has a bit-rate of 12 kbits/s.

The SAA2032 input is a time-multiplexed analog signal from the Read Amplifier. The signal contains ten time slots, of which nine are used. The Read Amplifier and the SAA2032 synchronize with the RDCLK and RDSYNC signals generated by the SAA2032.

Following A/D conversion and demultiplexing the nine channels are equalized. The encoding of the equalizing coefficients (12 per channel) are not fixed and must be loaded via the LT interface before operation.

The nine equalized output signals are up-sampled by a factor of 10 with the resulting signals fed to the slicer. The slicer output is applied to the SAA2022.

TEST

- A/D conversion
- Demultiplexing
- Equalization
- Zero crossing
- Eye-pattern.

Same as normal mode. In addition the digital and analog eye-pattern outputs are enabled. The eye-pattern output corresponds to one of the equalized channel outputs.

SEARCH

- A/D conversion
- Envelope detection
- Tape search and speed measurement.

In the search mode the analog input signal from the Read Amplifier is not the multiplexed signal but only the auxiliary channel signal.

Following A/D conversion the envelope of this signal is filtered and sliced. This forms the Alternating Envelope AENV output. The LABEL and VIRGIN outputs are detected from this and the tape search speed measured.

OFF

In the OFF mode the RDSYNC and RDCLK signals are HIGH, the EYE outputs are disabled and the channel and auxiliary outputs (CH0 to CH7 and AUX) are 3-stated.

Read Amplifier interface

The interface between the Read Amplifier and the SAA2032 consists of three signals:

1. VIN from Read Amplifier to SAA2032; time multiplexed data.
2. RDSYNC from SAA2032 to Read Amplifier; synchronization between Read Amplifier multiplexer and SAA2032 demultiplexer.
3. RDCLK from SAA2032 to Read Amplifier; data clock for Read Amplifier multiplexer.

The multiplexed VIN output of the Read Amplifier changes to another channel at the rising edge of RDCLK. RDSYNC synchronizes the Read Amplifier VIN output: if RDSYNC is HIGH, the rising edge of the RDCLK will select the AUX channel.

Figures 4 and 5 show the relationship between the SAA2032 and the Read Amplifier.

SAA2022 interface

The interface with the SAA2022 consists of the 9 data output signals CH0 to CH7, AUX.

Table 1 Dependency of Read Amplifier on operational mode.

OPERATIONAL MODE	RDSYNC	RDCLK
Normal	YES	YES
Test	YES	YES
Search	HIGH	YES
Off	HIGH	HIGH

Label and virgin detection interface

When the DCC player is in its search mode, the tape is fast-wound while the head retains tape contact. The SAA2032 can be made to operate in the search mode and the information will be read from the auxiliary tape track.

The following three signals are generated:

1. LABEL: label detection (HIGH if label is detected).
2. VIRGIN: virgin tape detection (HIGH if virgin tape is detected).
3. AENV: alternating envelope (sliced envelope).

AENV, LABEL and VIRGIN are disabled in normal or off modes. LABEL, VIRGIN and AENV are LOW.

AENV, LABEL and VIRGIN are enabled when the SAA2032 is in search mode.

The device detects the envelope AENV of the auxiliary track at search speeds between 3 and 50 times normal speed. If AENV is continuously HIGH (label detection), LABEL will be HIGH.

When AENV is continuously LOW (virgin tape detection) VIRGIN will be HIGH.
Figures 6, 7 and 8 show the relationship between AENV, VIRGIN and LABEL.

Labelled tape-speed calculation

When the DCC player is in its search mode, the tape speed increases. LABEL information is encoded throughout its length. To examine the length of a label, the tape speed must be known. In search mode the SAA2032 assesses the speed of labelled tapes. The microcontroller obtains this information via the LT-interface.

The speed information is encoded in 3 variables:

1. SVF Speed Validation Flag (HIGH if invalid).
2. SC (4..0) Speed counter.
3. SR (1..0) Speed Range.

$$\text{Search speed} = 2^{SR} \times \frac{51.2}{SC} \text{ x normal speed.}$$

If SC = 0 then search speed > 51.2.

With SR = 0, 1, 2 or 3 and SC = 0 to 31.

If SVF = 1 then SR and SC values are invalid.

Appendix 1 gives a table of the search mode speed control.

Microcontroller (LT) Interface

The SAA2032 is able to exchange information with the microcontroller via the LT-interface. The microcontroller performs as master, the SAA2032 as slave.

Figure 9 gives the operation of the LT-interface.

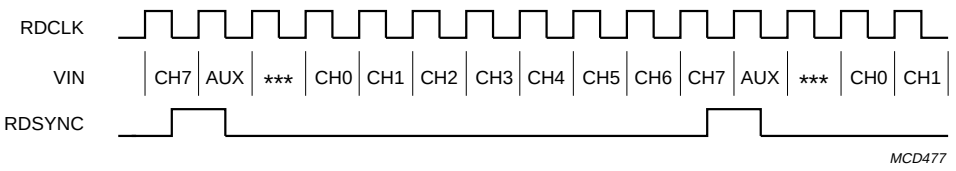
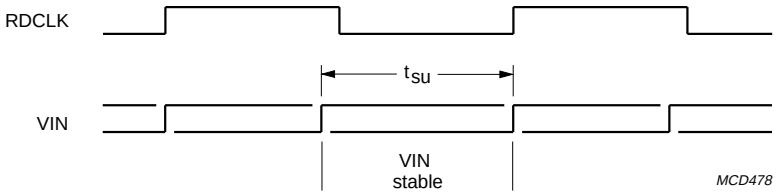


Fig.4 Signals on interface between Read Amplifier and SAA2032.

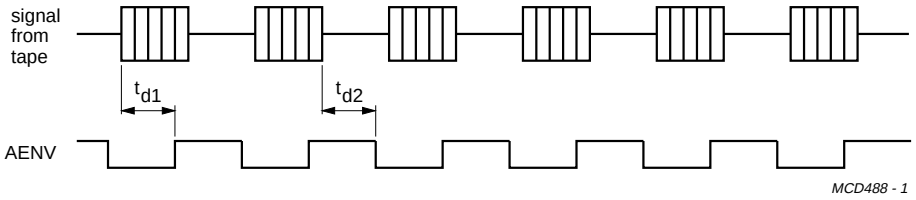


t_{su} > 80 ns; set-up time VIN before RDCLOCK HIGH.

Typical frequency for RDCLK = 3.072 MHz.

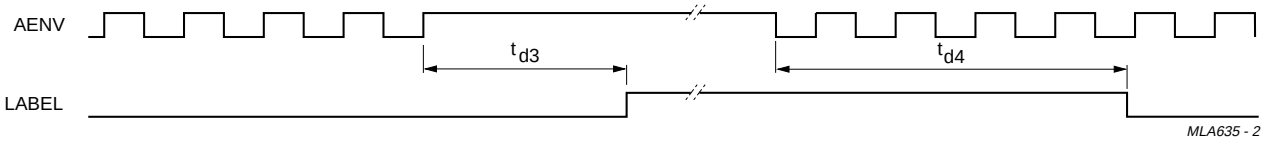
Typical frequency for RDSYNC = 307.2 kHz.

Fig.5 Timing.



$t_{d1} = t_{d2}$ = between 0.5 and 1.0 auxiliary block lengths.

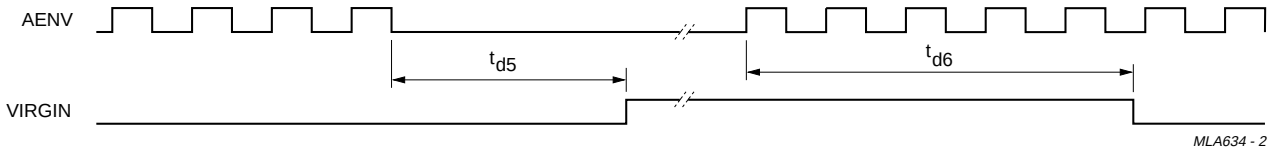
Fig.6 Diagram of AENV signal.



t_{d3} = between 4 and 12 auxiliary blocks.

t_{d4} = between 4 and 12 auxiliary blocks.

Fig.7 AENV and LABEL signals.



t_{d5} = t_{d6} = between 4 and 12 auxiliary blocks.

Fig.8 AENV and VIRGIN signals.

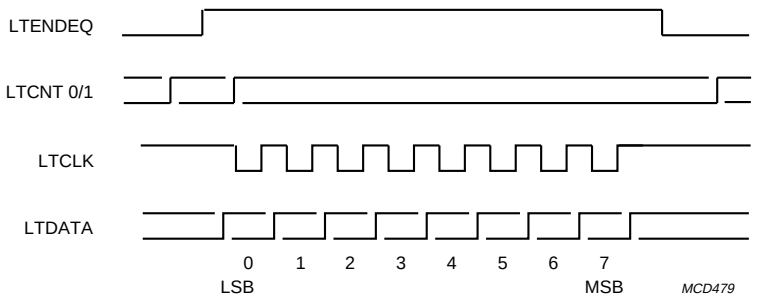


Fig.9 Typical operation of the LT-interface.

LTCNT specification

Table 2 Four types of data exchange performed on the interface.

LTCNT1	LTCNT0	LT DATA EXCHANGE MODE		FROM	TO
0	0	data	write	µC	DEQ
0	1	data	read	DEQ	µC
1	0	address	write	µC	DEQ
1	1	mode settings	write	µC	DEQ

Mode Settings Load (LTCNT = 11) (See Fig.10)

The 8-bits transmitted under 'mode settings load' control both the 'operation mode' and the 'data exchange type'.

Table 3 Mode settings; 'operation mode'.

a1	a0	OPERATION MODE
0	0	normal
0	1	test
1	0	search
1	1	off

Table 4 Mode settings; 'data exchange type'.

b1	b0	DATA	EXCHANGE	TYPE
0	0	write	coefficient	data
0	1	read	coefficient	data
1	1	read	envelope	data

Remark post condition: after every communication sequence the data exchange type must be set to "read coefficient data".

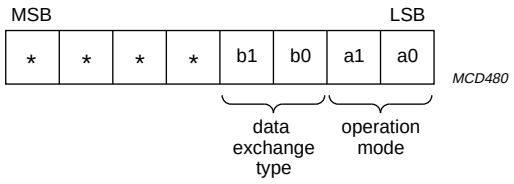


Fig.10 Mode settings load (LTCNT = 11).

Address Information Load (LTCNT = 10) (See Fig.11)

A channel/tap combination can be selected through this type of data exchange.

Co-efficient Data Load (LTCNT = 00) (See Fig.12)

This type of data exchange will overwrite the equalizer tap coefficient of the **current selected** channel/tap combination.

The coefficient data for tap <0000> of the auxiliary channel should always be zero.

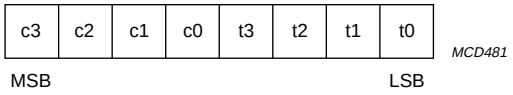
Data Read (LTCNT = 01) (See Fig.13)

This type of data exchange will send information from the LTDATA register in the SAA2032 to the microcontroller. Data in the LTDATA register depends upon the current data exchange type.

LTDATA interpretation:

- coefficient data: two's complement coefficient data
- tape speed data
  - d7 = SVF flag
  - d6 to d2 = SC4 to SC0
  - d1, d0 = SR1, SR0.

Tape speed data format is shown in Fig.14.



c3 to c0 --> channel number <0000 to 0111>
+ auxiliary channel <1000>
t3 to t0 --> tap number <0000 .. 1011>

Fig.11 Address information load (LTCNT = 10).

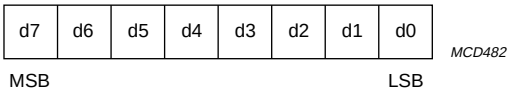


Fig.12 Coefficient data load (LTCNT = 00).

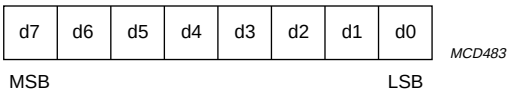


Fig.13 Read data (LTCNT = 01).

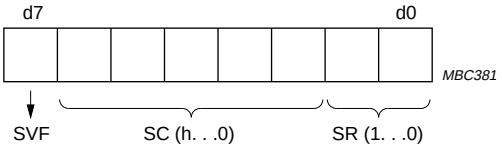
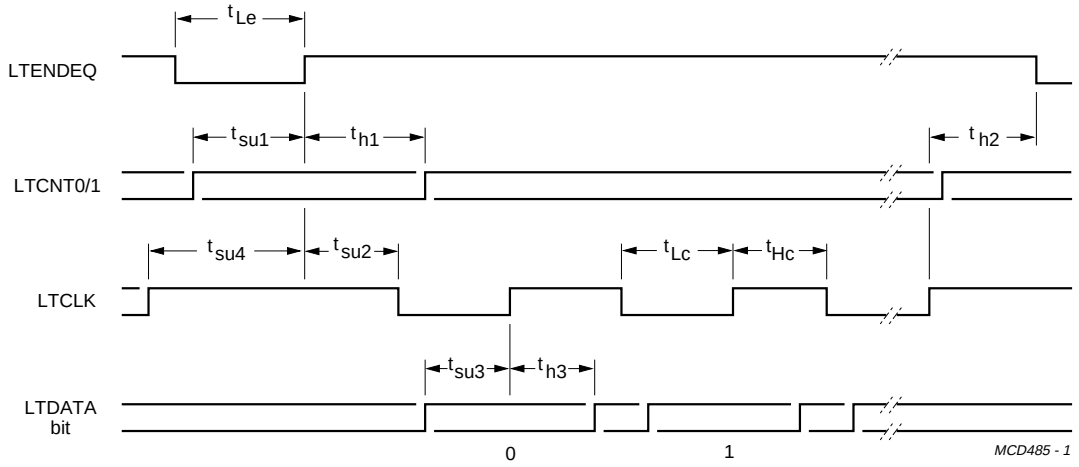


Fig.14 Tape speed data format.



t_{Le} > 120 ns; minimum LOW time LTENDEQ before transfer.

t_{su1} > 20 ns; set-up time LTCNT0/1 before LTENDEQ HIGH.

t_{h1} > 100 ns; hold time LTCNT0/1 after LTENDEQ HIGH.

$t_{su2} \geq 0$ ns; set-up time LTCNT0/1 before LTCLK LOW.

t_{h2} > 20 ns; hold time LTENDEQ after LTCLK HIGH.

t_{Lc} > 120 ns; minimum LOW time LTCLK.

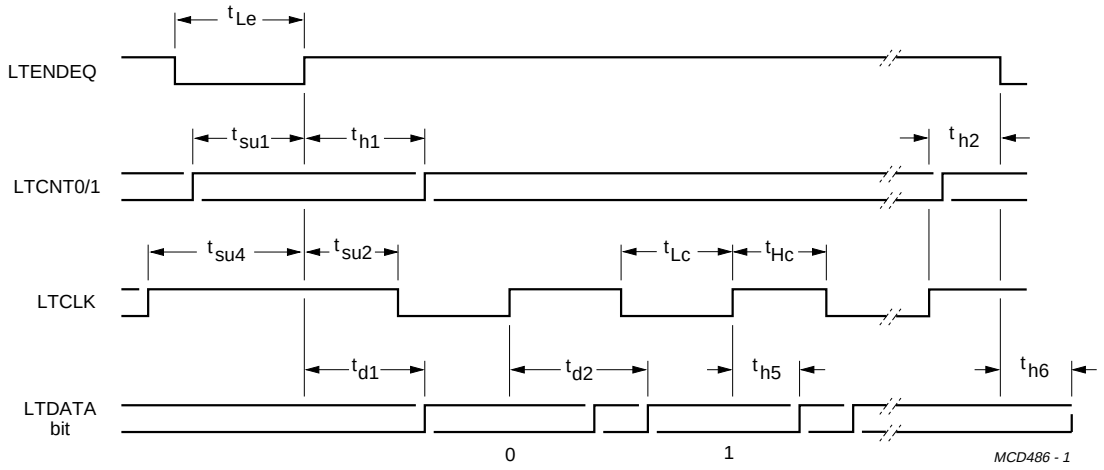
t_{Hc} > 120 ns; minimum HIGH time LTCLK.

t_{su4} > 200 ns; set-up time LTCLK before LTENDEQ HIGH.

t_{su3} > 100 ns; set-up time LTDATA before LTCLK HIGH.

t_{h3} > 20 ns; hold time LTDATA after LTCLK HIGH.

Fig.15 Microcontroller to SAA2032 timing.



t_{Le} > 120 ns; minimum LOW time LTENDEQ before transfer.

t_{su1} > 20 ns; set-up time LTCNT0/1 before LTENDEQ HIGH.

t_{h1} > 100 ns; hold time LTCNT0/1 after LTENDEQ HIGH.

$t_{su2} \geq 0$ ns; set-up time LTCNT0/1 before LTCLK LOW.

t_{h2} > 20 ns; hold time LTENDEQ after LTCLK HIGH.

t_{Lc} > 120 ns; minimum LOW time LTCLK.

t_{Hc} > 120 ns; minimum HIGH time LTCLK.

t_{su4} > 200 ns; set-up time LTCLK before LTENDEQ HIGH.

t_{d1} > 300 ns; maximum delay LTDATA after LTENDEQ HIGH.

t_{d2} > 400 ns; maximum delay LTDATA after LTCLK HIGH.

t_{h5} > 160 ns; hold time LTDATA after LTCLK HIGH.

t_{h6} > 0 ns; hold time LTDA after LTENDEQ LOW.

Fig.16 SAA2032 to Microcontroller timing.

Eye pattern output

To test equalization performance it is possible to output the equalized channels. For this purpose one analog and two digital output signals are provided. Selection of the EYE pattern output is determined by the last channel address sent to the SAA2032.

- DIGEYE: serial data line for 8-bits output value
- VAL: validation signal for data bits
- ANEYE: analog eye voltage output.

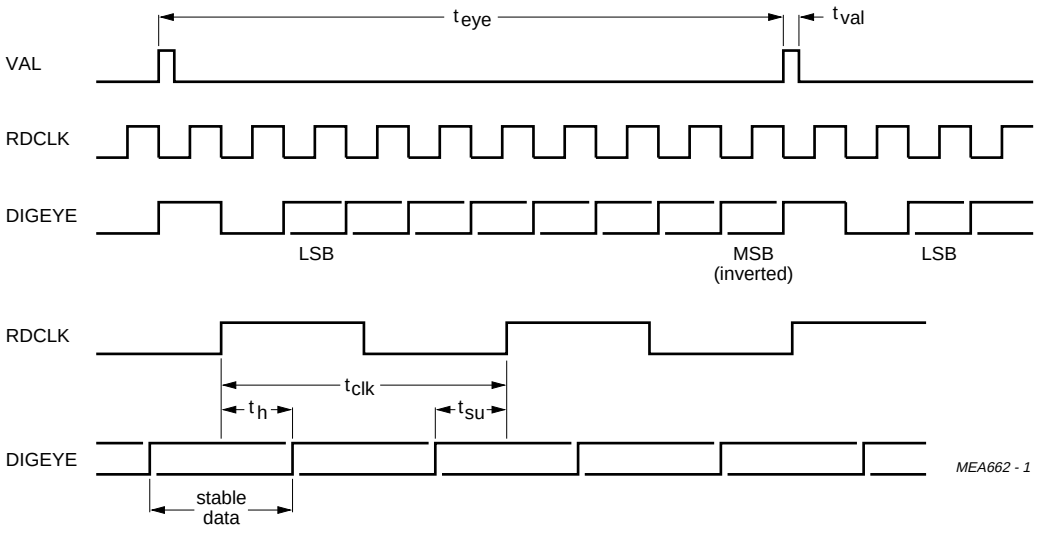
The eye outputs are enabled in test mode.

Table 5 Eye outputs.

OPERATION MODE	DIGEYE	ANEYE
Normal	LOW	HIGH
Test	ENABLED	ENABLED
Search	LOW	HIGH
Off	LOW	HIGH

The internal number representation in the SAA2032 is in two's complement. The format of the selected 8-bits will be converted to the off-set-binary format. This means that the MSB of the two's complement number has been inverted. This 8-bit number is shifted out via the DIGEYE output.

Figure 17 gives the eye pattern output timing.



t_{val} = 1/4 clock period; pulse width HIGH.

t_{su} > 60 ns; minimum set-up time data before clock.

t_h > 5 ns; minimum hold time data after clock.

$t_{clk} = 1/f_{clk}$.

f_{clk} = 3.072 MHz; nominal DIGEYE clock frequency.

$t_{eye} = 1/f_{eye}$.

f_{eye} = 307.2 kHz; nominal DIGEYE clock frequency.

Fig.17 Timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{SS}	supply current in V_{SS}		–	–100	mA
I_{DD}	supply current in V_{DD}		–	100	mA
I_I	input current		–10	10	mA
I_O	output current		–20	20	mA
P_{tot}	total power dissipation		–	550	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–1500	+1500	V
V_{es2}	electrostatic handling	note 3	–70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.8	5.0	5.5	V
V_{DDAD}	supply voltage for ADC	note 1	3.8	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; note 2	–	22	26	mA
		V_{DD} = 3.8 V; note 2	–	12	14	mA
I_{DDAD}	supply current for ADC	V_{DDAD} = 5 V	–	11	13	mA
		V_{DDAD} = 3.8 V	–	5	7	mA
I_{OP}	operating current	note 3	1.3	1.9	3.4	mA
Inputs f24, LTCLK, LTCNT0, LTCNT1 and LTENDEQ						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_I	input current	V_I = 0 V; T_{amb} = 25 °C	–	–	–10	µA
		V_I = V_{DD}; T_{amb} = 25 °C	–	–	10	µA
Input REFP						
V_{refp}	reference voltage		2.7	3.1	3.4	V
Input REFN						
V_{refn}	reference voltage		0.7	1.0	1.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs REFP and REFN						
ΔV_{ref}	reference voltage difference between REFP and REFN		2	2.1	2.7	V
Input VIN						
$V_{I(p-p)}$	input voltage (peak-to-peak)		V_{refn}	–	V_{refp}	V
I_I	input current		–	–	100	μA
Digital outputs						
V_{OL}	LOW level output voltage	note 4	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 4	V_{DD} – 0.5	–	–	V
Output ANEYE						
V_O	output voltage	note 4	–	–	V_{DDAD}	V
V_O	output voltage range	note 4	–	1.1	–	V
Input/output LTDATA						
V_{OL}	LOW level output voltage	I_O = –3 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
I_{OZ}	leakage current with outputs in 3-state	V_I = 0 V; T_{amb} = 25 °C	–	–	10	μA
		$V_I = V_{DD}$; T_{amb} = 25 °C	–	–	10	μA
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V

Notes

1. V_{DDAD} should never be lower than V_{DD} – 0.2 V.
2. For load impedances in a typical application circuit.
3. Operating reference current for the specified range of V_{refp} allowing for the tolerance on the internal resistor.
4. For outputs DIGEYE, RDSYNC, RDCLK, CH0 to CH7, AUX and VAL the maximum load current is 1 mA. For ANEYE output the maximum load current is 10 μA. For VIRGIN, LABEL and AENV the maximum load current is 2 mA.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIN						
C_i	input capacitance		–	–	15	pF
All digital inputs						
C_i	input capacitance		–	–	10	pF
Clock input f24						
f	clock frequency		23	24.576	26	MHz
t_p	pulse width LOW or HIGH		10	–	–	ns
Inputs LTCLK, LTENDEQ, LTCNT0 and LTCNT1						
t_{su}	set-up time to f24	note 1	10	–	–	ns
t_h	hold time from f24	note 1	30	–	–	ns
All outputs						
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	50	pF
t_d	propagation delay time from f24	note 1	–	–	80	ns
Input/output LTDATA						
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	50	pF
t_d	propagation delay time from f24		–	–	80	ns
t_{su}	set-up time to f24	note 1	10	–	–	ns
t_h	hold time from f24	note 1	30	–	–	ns

Note

1. LOW-to-HIGH transition.

CONVERTER CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-Digital Converter; VIN						
	resolution		–	7	–	bits
	conversation data available after		–	$2 \times t_{cy}$	–	
	effective input bandwidth	6-bit resolution at f_s = 3.1 MHz	0.5	–	–	MHz
	differential non-linearity		–	–	±0.99	LSB
V_{refn}	reference voltage at VREFN	note 1	0.7	1.0	1.4	V
V_{refp}	reference voltage at VREFP		2.7	3.1	3.4	V
ΔV_{ref}	reference voltage difference between REFP and REFN		2	2.1	2.7	V
V_i	input voltage		V_{refn}	–	V_{refp}	V
S+THD/N	signal-to-total harmonic distortion and noise ratio	note 2	21	–	–	dB
C_i	input capacitance		–	–	15	pF
I_I	input current (DC)	note 3	–	–	100	µA
Digital-to-analog converter; output ANEYE						
	resolution		–	6	–	bits
V_O	output voltage	note 4	–	–	V_{DDAD}	V
V_O	output voltage range	note 4	–	1.1	–	V

Notes

1. V_{refp} is supplied externally.
   V_{refn} is derived internally and set to $^1/_3V_{refp}$.
   V_{refn} must be decoupled externally at pin 6 via a 100 nF capacitor.
2. Signal level (f_s) –20 dB, at any DC level within the input voltage range.
3. The output impedance of the analog input signal source must be <150 Ω.
4. Load impedance ≥1 MΩ.

APPENDIX 1

Search Mode Speed Control Interface

In search mode the SAA2032 measures the tape speed. The tape speed is encapsulated in the variables:

- SVF Speed Validation Flag; is HIGH if NOT valid
- SC Speed Counter
- SR Speed Range.

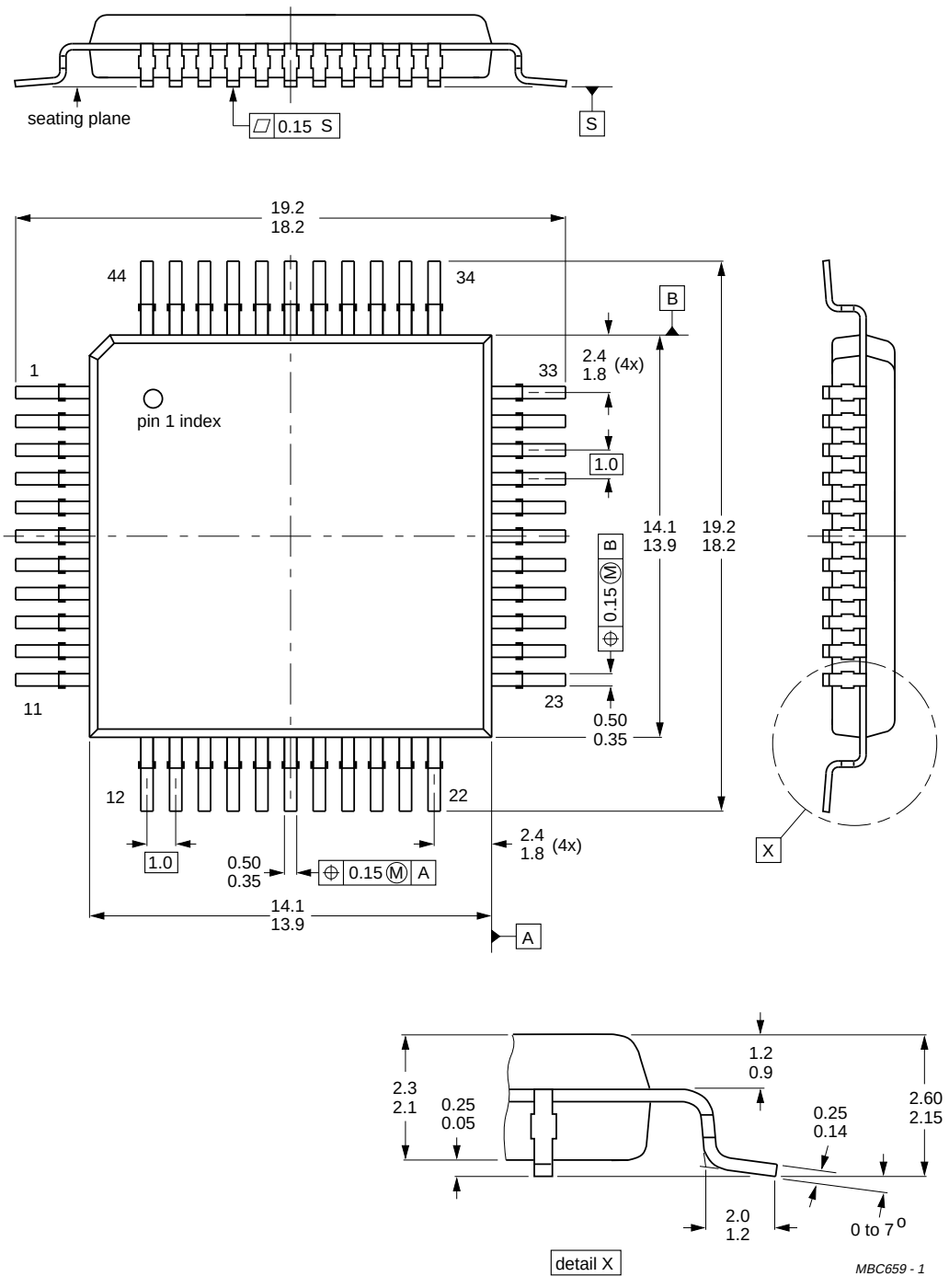
The values in Table 6 represent the speed in multiples of the nominal tape speed of 4.76 cm/s.

Table 6 Speed in multiples of nominal tape speed.

SC[4 .. 0]	SR[1 .. 0]				REMARKS
	0	1	2	3	
0	>51.20	>102.40	>204.80	>409.60	shift to higher speed range
1	51.20	102.40	204.80	409.60	
2	25.60	51.20	102.40	204.80	
3	17.07	34.13	68.27	136.53	
4	12.80	25.60	51.20	102.40	
5	10.24	20.48	40.96	81.92	
6	8.53	17.07	34.13	68.27	
7	7.31	14.63	29.26	58.51	
8	6.40	12.80	25.60	51.20	normal working area
9	5.69	11.38	22.76	45.51	
10	5.12	10.24	20.48	40.96	
11	4.65	9.31	18.62	37.24	
12	4.27	8.53	17.07	34.13	
13	3.94	7.88	15.75	31.51	
14	3.66	7.31	14.63	29.26	
15	3.41	6.83	13.65	27.31	
16	3.20	6.40	12.80	25.60	
17	3.01	6.02	12.05	24.09	

SC[4 .. 0]	SR[1 .. 0]				REMARKS
	0	1	2	3	
18	2.84	5.69	11.38	22.76	shift to lower speed range
19	2.69	5.39	10.78	21.56	
20	2.56	5.12	10.24	20.48	
21	2.44	4.88	9.75	19.50	
22	2.33	4.65	9.31	18.62	
23	2.23	4.45	8.90	17.81	
24	2.13	4.27	8.53	17.07	
25	2.05	4.10	8.19	16.38	
26	1.97	3.94	7.88	15.75	
27	1.90	3.79	7.59	15.17	
28	1.83	3.66	7.31	14.63	
29	1.77	3.53	7.06	14.12	
30	1.71	4.41	6.83	13.65	
31	1.65	3.30	6.61	13.21	

PACKAGE OUTLINE



Dimensions in mm.

Fig.18 44-lead quad flat-pack; plastic (SOT205AG).

SOLDERING

Quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two waves (dual-wave), in which, in a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
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NOTES

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